

University of Bahrain
College of Information technology
Department of Computer Engineering

Test (2)

Course Title: Digital Logic
Course number: ITCE 202
Semester: 1
Academic Year: 2007/2008
Duration : 1 hour 15 minutes
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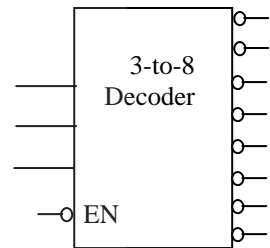
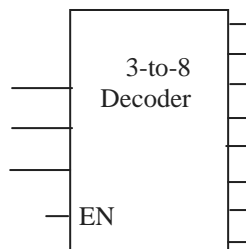
Question [1]: (15 Mark)

Implement the following Boolean function:

$$f(A, B, C) = \sum m(1, 3, 4, 6)$$

Using a 3-to-8 line decoder and:

- a. OR gate.
- b. NAND gate.
- c. AND gate.
- d. NOR gate.

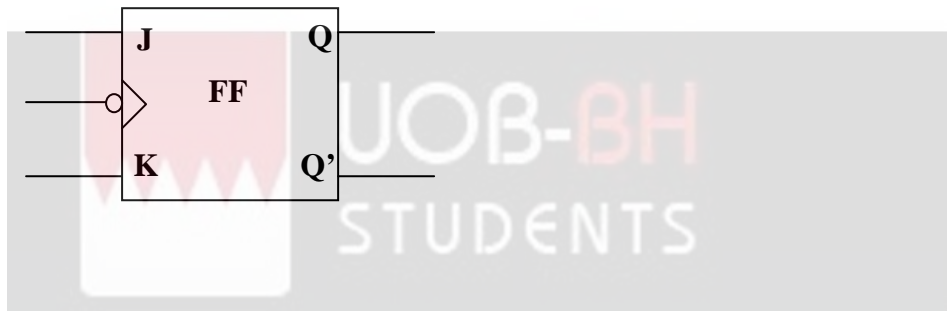


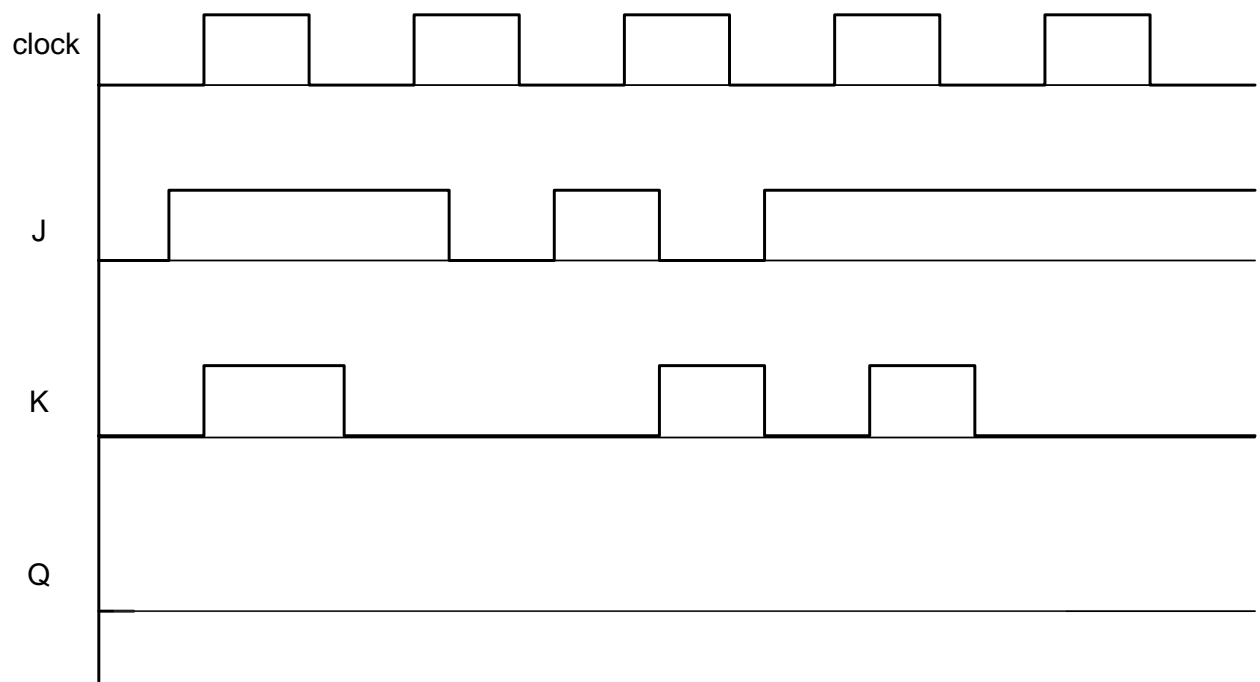
Question [2]: (25 Marks)

- a. Design a 3-bit counter using T-flip-flops and logic gates which counts in the sequence: 001, 100, 101, 111, 110, 010, 011, and repeat. (Do not draw the circuit, just give the equations).
- b. What will happen if the counter is started in state 000, draw the complete state graph.

Question [3]: (10 Marks)

Complete the timing diagram for the given Flip-Flop.





Question [4]: (15 Mark)

A circuit has four inputs RSTU and four outputs VWYZ. RSTU represents a Binary-Coded-Decimal digit. VW represent the quotient and YZ the remainder when RSTU is divided by 3 (VW and YZ represent 2-bit binary numbers). Assume that invalid inputs do not occur. Realize the circuit using a ROM by deriving its truth table and drawing the ROM as a block stating its size, inputs and outputs.

Question [5]: (20 Mark)

Design a combinational logic circuit that detects an error in the representation of decimal digits in BCD. In other words, obtain a logic diagram whose output is equal 1 when the inputs contain any one of the six unused bit combinations in the BCD code. As follows:

- Construct the truth table.
- Realize the expression using 8-to-1 multiplexer with no added gates.
- Realize the expression using 4-1 multiplexer with added gates if required.



Question [6]: (15 Mark)

A shift register is described by the given table. The shift register is connected as shown in the figure below. Complete the timing diagram for Q_A , Q_B , Q_C , Q_D assume initial value of 0.

Sh	Ld	Q_A^+	Q_B^+	Q_C^+	Q_D^+
0	0	Q_A	Q_B	Q_C	Q_D
0	1	D_A	D_B	D_C	D_D
1	x	SI	Q_A	Q_B	Q_C

